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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,310	09/11/2003	Richard L. Coulson	ITL.1029US (P16765)	5388

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EXAMINER	
BHAT, ADITYA S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,310	COULSON ET AL.	
	Examiner	Art Unit	
	Aditya S. Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42 and 46-59* is/are pending in the application.

4a) Of the above claim(s) *43-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,12-19,21,26-29,33-42,46-49 and 51-59* is/are rejected.

7)☐ Claim(s) *5,10,11,20,22-25,30-32 and 50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/11/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 13, 26, and 35 are objected to because of the following informalities: The above mentioned claims recite the limitation "the temperature" in lines 2, 4, 5 and 2 respectively. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,6-9,12-19, 21,26-29, 33-42, 46-49, and 51-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (USPN 5,598,395) in view of Neufeld (USPN 5,974,438).

With regards to claims 1 and 13, Watanabe (USPN 5,598,395) teaches a method comprising, or an article comprising a medium storing instructions that, if executed, enable a processor based system to

monitoring a temperature; (S1;figure 3) and

in response to a detection of a temperature condition (S4;figure 3), transitioning the cache memory from a write-back cache to a write-through cache. (S8A; figure 3)

With regards to claim 3, Watanabe (USPN 5,598,395) teaches adjusting the operation of a system using said memory at a first temperature and, in response to the

detection of a higher, second temperature, transitioning the cache from a write-back cache to a write-through cache. (Col.6, lines 1-8).

With regards to claims 4 and 49, Watanabe (USPN 5,598,395) teaches slowing an operation of said system at said first temperature. (S9; figure 3)

With regards to claim 6, Watanabe (USPN 5,598,395) teaches adjusting what data is cached based on a detection of said first temperature. (S9; figure 3)

With regards to claim 7 and 16, Watanabe (USPN 5,598,395) teaches shutting off the said cache memory at a temperature above said second temperature. (Col. 6, lines 1-8).

With regards to claim 8, Watanabe (USPN 5,598,395) teaches monitoring for a temperature lower than said second temperature. (S4; figure 3)

With regards to claim 9, Watanabe (USPN 5,598,395) teaches upon detecting a lower temperature, resuming operation of said cache memory. (Figure 3)

With regards to claims 12 and 17, Watanabe (USPN 5,598,395) teaches flushing a cache line in said cache memory that has not been written through to a source memory. (S8A; Figure 3-4)

With regards to claim 15, Watanabe (USPN 5,598,395) teaches storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache. (Col.5, lines 11-65)

With regards to claim 18, Watanabe (USPN 5,598,395) teaches a processor based system to monitor for a temperature lower than said second temperature. (s4; figure 3-4)

With regards to claim 19, Watanabe (USPN 5,598,395) teaches a processor based system to resume operation of said cache memory upon detecting a lower temperature. (s4; figure 3-4)

With regards to claim 21, Watanabe (USPN 5,598,395) teaches a processor-based system to shut off the cache and invalidate all the cache lines. (S9; figure 3)

With regards to claim 26, Watanabe (USPN 5,598,395) teaches a processor-based system comprising:

a processor; (6;figure 1)

a disk drive coupled to said processor; (10, 20;figure 1)

a cache memory coupled said processor; (9;figure 1) and

a storage(8;figure 1) to store a cache driver to monitor a temperature and in response to the detection of a temperature condition, transition the cache memory from a write-back cache memory to a write-through cache memory(S8A;figure 3).

With regards to claim 29, Watanabe (USPN 5,598,395) teaches storing instructions that enable a dirty line to be flushed. (S8A; figure 3-4)

With regards to claim 33, Watanabe (USPN 5,598,395) teaches a storage, stores instructions that enable the system to resume cache operations after shutting off the cache memory in response to a cache condition by initially resuming reduced speed operations in a first stage and thereafter resuming normal operations. (8;figure 1)

With regards to claim 34, Watanabe (USPN 5,598,395) teaches a cache memory includes a temperature sensor. (14; figure 1)

With regards to claim 35, Watanabe (USPN 5,598,395) teaches a circuit comprising:

a component to receive an indication of a temperature (14;figure 1) and to develop a signal to transition the cache memory from a write-back cache to a write-through cache in response to said temperature indication. (S7-s8A; figure 3)

With regards to claim 36, Watanabe (USPN 5,598,395) teaches a component to vary the operation of a system to adjust for the temperature affected operation of said cache memory. (figure 3)

With regards to claim 37, Watanabe (USPN 5,598,395) teaches a component to adjust a caching operation of the system in response to a temperature indication from said memory. (figure 3)

With regards to claim 38-39, Watanabe (USPN 5,598,395) teaches a component to shut off said cache in response to a temperature indication. (S9; figure 4)

With regards to claim 46, Watanabe (USPN 5,598,395) teaches a method comprising:

monitoring a temperature; (s1;figure 3-4) and

in response to a detection of a temperature condition, operating a cache memory in one of two different modes depending on the temperature. (s12, s8A; figure 4)

With regards to claim 48, Watanabe (USPN 5,598,395) teaches the operation of a system using said memory at a first temperature and, in response to the detection of a

higher, second temperature, transitioning the cache from a write-back cache to a write-through cache. (S7, S8A; figure 3)

With regards to claim 51, Watanabe (USPN 5,598,395) teaches a computer readable medium storing instructions that, if executed, enable a processor-based system to:

monitor a temperature of a cache memory; (s1; figure 3) and

in response to the detection of a temperature condition, operating a cache memory in one of two different modes depending on the temperature. (S12, S8A; figure 4)

With regards to claim 53, Watanabe (USPN 5,598,395) teaches a storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache. (S7, S11, S12, S8A; figure 4)

With regards to claim 54, Watanabe (USPN 5,598,395) teaches a circuit comprising:

a cache memory; (9; figure 1) and

a component to receive an indication of a temperature (figure 3) and to develop a signal to transition the cache memory from a first to a second operating mode in response to said temperature indication. (S7, S8A; figure 3)

With regards to claim 55, Watanabe (USPN 5,598,395) teaches a component to vary the operation of a system to adjust for the temperature affected operation of said cache memory. (S7, s8a; figure 3)

With regards to claim 56, Watanabe (USPN 5,598,395) teaches component to adjust a caching operation of the system in response to a temperature indication from said memory. (S7, S8a; figure 3)

With regards to claim 57, Watanabe (USPN 5,598,395) teaches a component to shut off said cache in response to a temperature indication. (s9; figure 3)

With regards to claim 58, Watanabe (USPN 5,598,395) teaches component to invalidate a cache line in said cache memory. (S9; figure 3)

With regards to claim 2, 14, 27-28, 34, 40-42, 47, 52 and 59 Watanabe (USPN 5,598,395) does not appear to explicitly disclose monitoring the temperature of a ferroelectric polymer cache memory; a cache memory is a flash memory.

Gudesen et al. (WO 2004/025658) discloses monitoring the temperature of a ferroelectric polymer cache memory, a cache memory includes a temperature sensor. (Page 9, lines 29-30)

It would have been obvious to one skilled in the art at the time of the invention to modify Watanabe (USPN 5,598,395) with Gudesen et al. (WO 2004/025658) to include a temperature sensor to monitor a ferroelectric polymer cache memory in order to determine at least one parameter indicative of a change in the memory cell. (Page 9, lines 9-10).

Allowable Subject Matter

3. The following is a statement of reasons for the indication of allowable subject matter: Claims 5, 10-11, 20, 22-25 30-32 and 50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 5,10-11, 20, 22-25, 30-32 and 50:

The primary reason for the allowance of claim 5 and 50 is the inclusion of the method steps of: reducing prefetching at said first temperature. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claims 10 and 20 is the inclusion of the method steps of: waiting for a power cycle before resuming cache operations. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 11 is the inclusion of the method steps of: shutting off said cache memory and invalidating cache lines in said cache memory. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 22 is the inclusion of: processor-based system to transition the cache memory from a write-back to cache to a write-

through cache memory at a first, higher temperature and to adjust for the slower speed of the cache memory at a second temperature lower than said first temperature. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

The primary reason for the allowance of claim 30 is the inclusion of the method steps of: instructions that enable the system to adjust for reduced speed operation at a first temperature, switch to a write-through cache memory at a second higher temperature, and invalidate cache lines and shut off the cache memory at still a higher temperature. It is this feature found in the claim, as it is claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Claims 23-25 are allowed due to their dependency on claim 22.

Claims 31-32 are allowed due to their dependency on claim 30.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

4. Applicant's arguments filed 8/1/2005 have been fully considered but they are not persuasive.

Applicant is reminded that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allowed. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

In this instance applicant argues that the prior art of record does not teach transitioning between write back and write through cache.

Write back cache is when data is written to the cache and transferred to the main memory when absolutely necessary. Write through cache is when the data is written to both the cache and to the main memory.

The pending application teaches transitioning between write back to write through cache in response to a temperature condition.

Transitioning is defined as the act of passing from one state to the next. The prior art of record teaches the data is passed between the write back cache to the main

memory (S8A; figures 3-4). Therefore, the claimed invention is believed to read on the prior art of record.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Martinez Jr. et al. (USPN 5,860,111) coherency for write back cache in a system designed for write through cache including exporting on hold, Martinez Jr. et al. (USPN 5,664,149) teaches coherency for write back cache in a system designed for write through cache including an export/ invalidate protocol, Martinez Jr. et al. (USPN 5,524,234) teaches coherency for write back cache in a system designed for write through cache including write back control.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
October 16, 2005

BRYAN BUI
PRIMARY EXAMINER

10/24/05